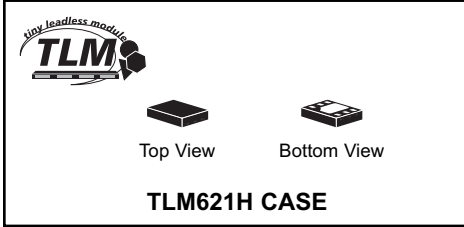




CTLDM7120-M621H

**SURFACE MOUNT TLM™  
N-CHANNEL  
ENHANCEMENT-MODE  
SILICON MOSFET**



# Central™ Semiconductor Corp.

**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CTLDM7120-M621H is an Enhancement-mode N-Channel Field Effect Transistor, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. This MOSFET offers Low  $r_{DS(ON)}$  and Low Threshold Voltage.

**MARKING CODE: CNH**

**FEATURES:**

- Device is **Halogen Free** by design
- Device is **RoHS** compliant
- ESD protection up to 2kV
- Low  $r_{DS(ON)}$  (0.25Ω MAX @  $V_{GS}=1.5V$ )
- High current ( $I_D=1.0A$ )
- Logic level compatibility

**APPLICATIONS:**

- Load/Power switches
- Power supply converter circuits
- Battery powered portable equipment

**MAXIMUM RATINGS:** ( $T_A=25^\circ C$ )

Drain-Source Voltage  
 Gate-Source Voltage  
 Continuous Drain Current (Steady State)  
 Maximum Pulsed Drain Current ( $t_p=10\mu s$ )  
 Power Dissipation (Note 1)  
 Operating and Storage Junction Temperature  
 Thermal Resistance (Note 1)

**SYMBOL**

$V_{DS}$  20  
 $V_{GS}$  8.0  
 $I_D$  1.0  
 $I_{DM}$  4.0  
 $P_D$  1.6  
 $T_J, T_{stg}$  -65 to +150  
 $\theta_{JA}$  75

**UNITS**

V  
 V  
 A  
 A  
 W  
 $^\circ C$   
 $^\circ C/W$

**ELECTRICAL CHARACTERISTICS:** ( $T_A=25^\circ C$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{GSSF}, I_{GSSR}$	$V_{GS}=8.0V, V_{DS}=0V$			10	$\mu A$
$I_{DSS}$	$V_{DS}=20V, V_{GS}=0V$			10	$\mu A$
$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
$V_{GS(th)}$	$V_{DS}=10V, I_D=1.0mA$	0.5		1.2	V
$V_{SD}$	$V_{GS}=0V, I_S=1.0A$			1.1	V
$r_{DS(ON)}$	$V_{GS}=4.5V, I_D=0.5A$		0.075	0.10	$\Omega$
$r_{DS(ON)}$	$V_{GS}=2.5V, I_D=0.5A$		0.10	0.14	$\Omega$
$r_{DS(ON)}$	$V_{GS}=1.5V, I_D=0.1A$		0.17	0.25	$\Omega$
$g_{FS}$	$V_{DS}=10V, I_D=0.5A$		4.2		S
$C_{rss}$	$V_{DS}=10V, V_{GS}=0, f=1.0MHz$		45		pF
$C_{iss}$	$V_{DS}=10V, V_{GS}=0, f=1.0MHz$		220		pF
$C_{oss}$	$V_{DS}=10V, V_{GS}=0, f=1.0MHz$		120		pF

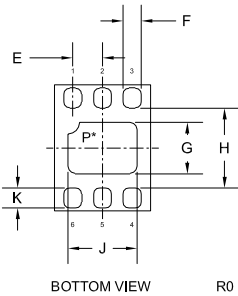
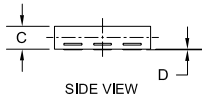
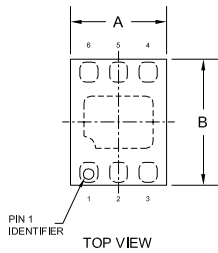
Notes: (1) Mounted on a 4-layer JEDEC test board with one thermal vias connecting the exposed thermal pad to the first buried plane. PCB was constructed as per JEDEC standards JESD51-5 and JESD51-7.

R1 (15-January 2009)

**ELECTRICAL CHARACTERISTICS - Continued:** ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$t_{on}$	$V_{DD}=10\text{V}$ , $V_{GS}=5.0\text{V}$ , $I_D=0.5\text{A}$		25		ns
$t_{off}$	$V_{DD}=10\text{V}$ , $V_{GS}=5.0\text{V}$ , $I_D=0.5\text{A}$		140		ns

**TLM621H CASE - MECHANICAL OUTLINE**

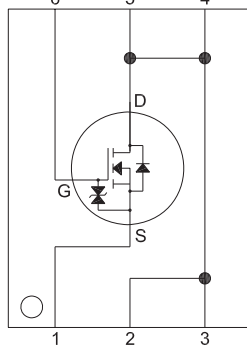


Exposed pad P internally connected to pins 3 and 4

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.065	1.35	1.65
B	0.073	0.085	1.85	2.15
C	0.012	0.016	0.30	0.40
D	0.000	0.002	0.00	0.05
E	0.020		0.50	
F	0.008	0.012	0.20	0.30
G	0.027	0.035	0.69	0.89
H	0.053	0.057	1.35	1.45
J	0.039	0.047	0.99	1.19
K	0.011	0.015	0.28	0.38

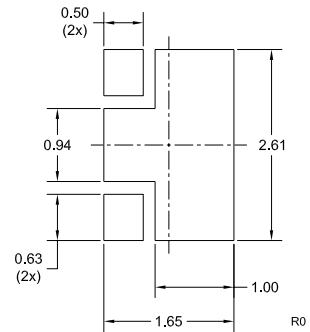
TLM621H (REV:R0)

**PIN CONFIGURATION  
TOP VIEW**



**MARKING CODE: CNH**

**Optional Mounting Pads  
(Dimensions in mm)**



For standard mounting refer to TLM621H Package Details

**LEAD CODE:**

- 1) SOURCE
- 2) DRAIN
- 3) DRAIN
- 4) DRAIN
- 5) DRAIN
- 6) GATE